ABSTRACT OF THE DISCLOSURE

A method is provided for forming a highly dense stacked gate flash memory cell with a structure having multi floating gates that can assume 4 states and, therefore, store 2 bits at the same time. This is accomplished by providing a semiconductor substrate having gate oxide formed thereon, and shallow trench isolation and a p-well formed therein. A layer of nitride is next formed over the substrate and an opening formed therein. Polysilicon floating gate spacers are formed in the opening. A dielectric layer is then formed over the floating gates followed by the forming of a control gate. The adjacent nitride layer is then removed leaving a multi-level structure comprising a control gate therebetween multi floating gates with the intervening dielectric layer.